



PATENT APPLICATION
Docket No. 9903-014

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jong-Kon Choi Conf. No.: 5622
Serial No. 09/847,620 Examiner: James M. Mitchell
Filed: May 2, 2001 Art Unit: 2827
For: METHOD FOR MANUFACTURING DIGITAL
MICRO-MIRROR DEVICE (DMD) PACKAGES

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR
ALLOWANCE**

Applicant submits that the prior art alone or in combination does not teach a method for manufacturing a semiconductor package, said method comprising:

providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface, and having one or more mirrors formed on the active surface and a plurality of bond pads formed on a periphery of the chip;

forming a photoresist over the one or more mirrors;

singulating the one or more semiconductor chips from the wafer;

attaching the back surface of the one or more semiconductor chip to a top surface of a base substrate;

electrically interconnecting the bond pads of the semiconductor chip to the base substrate;
and

removing the photoresist from the semiconductor chips after the electrically interconnecting the bond pads to the base substrate, as recited in allowed claim 1.

Applicant submits that the prior art alone or in combination does not teach a method for manufacturing digital micro-mirror device (DMD) packages, said method comprising:

providing a wafer including a plurality of DMD semiconductor chips, each chip comprising an active surface and a back surface and having one or more mirrors formed on substantially the center of the active surface of the chip, a plurality of electrode pads formed on the periphery of the active surface;

forming a photoresist over the mirrors;
forming a metallic layer on a back surface of the wafer;
separating the wafer into the individual semiconductor chips;
attaching the back surface of each semiconductor chip to an upper surface of a base substrate using a metallic adhesive;
interconnecting the electrode pads of the semiconductor chip to the base substrate with one or more bonding wires;
removing the photoresist from the semiconductor chips after interconnecting the electrode pads to the base substrate;
forming an anti-sticking film on the active surface of the semiconductor chip for protecting the semiconductor chips from dust and moisture; and
hermetically sealing the semiconductor chip and the bonding wires on the upper surface of the base substrate, as recited in allowed claim 5.

Applicant submits that the prior art alone or in combination does not teach a method for manufacturing a semiconductor package, said method comprising:

providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface and having one or more mirrors and electrodes formed on the active surface;
coating the one or more mirrors with a photoresist film;
singulating the one or more semiconductor chips from the wafer;
attaching the back surface of the one or more semiconductor chip to a top surface of a base substrate using a metallic adhesive;
electrically interconnecting the electrodes of the semiconductor chip to the base substrate;
and
removing the coated photoresist film from the one or more mirrors of the semiconductor chips after the interconnection, as recited in allowed claim 16.

Applicant submits that the prior art alone or in combination does not teach a method for manufacturing a semiconductor package, said method comprising:

providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface, and having one or more mirrors formed on the active surface and a plurality of bond pads formed on a periphery of the chip;
forming a photoresist over the one or more mirrors;
forming a metallic layer over a back surface of the wafer;
singulating the one or more semiconductor chips from the wafer;
attaching the back surface of the one or more semiconductor chip to a top surface of a

base substrate using a metallic adhesive;

electrically interconnecting the bond pads of the semiconductor chip to the base substrate;
and

removing the photoresist from the semiconductor chips after the electrically interconnecting the bond pads to the base substrate, as recited in allowed claim 20.

Applicant submits that the prior art alone or in combination does not teach a method for manufacturing digital micro-mirror device (DMD) packages, said method comprising:

providing a wafer including a plurality of DMD semiconductor chips, each chip comprising an active surface and a back surface and having one or more mirrors formed on substantially the center of the active surface of the chip, a plurality of electrode pads formed on the periphery of the active surface;

forming a photoresist over the mirrors;

forming a metallic layer on a back surface of the wafer;

separating the wafer into the individual semiconductor chips;

attaching the back surface of each semiconductor chip to an upper surface of a base substrate using a metallic adhesive;

interconnecting the electrode pads of the semiconductor chip to the base substrate with one or more bonding wires;

removing the photoresist from the semiconductor chips after interconnecting the electrode pads to the base substrate;

forming an anti-sticking film on the active surface of the semiconductor chip for protecting the semiconductor chips from dust and moisture; and

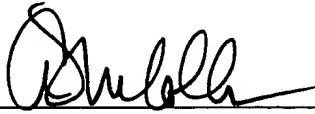
hermetically sealing the semiconductor chip and the bonding wires on the upper surface of the base substrate at a predetermined temperature not higher than the temperature on which said attaching the semiconductor chip to the base substrate is performed, as recited in allowed claim 21.

The remaining claims further distinguish over the prior art.

Customer No. 20575

Respectfully submitted,

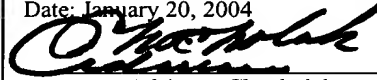
MARGER JOHNSON & McCOLLOM, P.C.



Alan T. McCollom
Reg. No. 287,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

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Adrienne Chocholak



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TRANSMITTAL LETTER

Enclosed for filing in the above-referenced application are the following:

- ☒ Applicant's Comments on Examiner's Statement of Reasons for Allowance
- ☒ Publication and Issue Fee
- ☒ In connection with issuance of a patent:
 - ☐ Supplemental Declaration ☒ PTO Form 85B
- ☒ PTO Form 2038 authorizing credit card payment of \$1630.00, issue fee (\$1330.00) and publication fee (\$300.00) is enclosed.
- ☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

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Adrienne Chocholak